REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed September 17, 2003. In the Office Action, the Examiner rejected claims 1-5 and 11-15 under 35 U.S.C. §102(b); and claims 6-10 and 16-30 under 35 U.S.C. §103(a). Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102(b)

In the Office Action, the Examiner rejected claims 1-5 and 11-15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,996,061 issued to Lopez-Aguado et al. ("Lopez-Aguado"). Applicants respectfully traverse the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of anticipation.

Applicants reiterate the arguments set forth in the previously filed Response to the Office Action.

1) The Examiner has not met the burden of proof to show inherency of a gating circuit.

In the Office Action, the Examiner states that "[a]pplicant argue that a process that needs to be terminated based on the presence of a variable in storage does not inherently require a gating circuit. Examiner disagrees and suggests that Applicant is attempting to read limitations into the claim that do not exist; as stated previously a circuit which passes or does not pass a signal (to terminate) based upon a control input (based on the proper address), is required to achieve the termination of prefetching based upon an address being found in the queue." Applicants respectfully disagree. The Examiner's argument is circular.

Claims 1, 11, and 21 recite at least two elements: (1) the access request matches to at least P of the stored prefetch addresses, and (2) a gating circuit to disable the access request.

In the rejecting claims 1, 11, and 21 under 35 U.S.C. §102(b), the Examiner cited Lopez-Aguado and argued that a gating circuit is inherent to terminate prefetching based upon the determination that an address is in the prefetch queue. In disputing this conclusion, Applicants argue that even assuming that a process is terminated based on the presence of a variable in storage, this termination does not inherently require a gating circuit. The Examiner now states

that Applicant is attempting to read limitations into the claim that do not exist. The scenario may be summarized as below.

Examiner: Although element X is not explicitly present in the reference, but it is inherently required by the process Z disclosed in the reference.

Applicant: No, the process Z does not inherently require element X.

Examiner: Applicant is attempting to read limitations into the claim.

The above indicates that the Examiner's argument is circular. The Examiner has a burden of proof to provide a rationale of inherency. The Examiner has not met that burden, because the Examiner has not shown how a termination of prefetching inherently requires a gating circuit. In the previous response, Applicant argues that the Examiner's inherency reasoning is flawed because "it does not identify the signal to be gated and the output signal of the gating circuit (if indeed it is required)". The Examiner must provide rationale or evidence tending to show inherency (MPEP 2112). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) "In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

The Examiner apparently misapplies the inherency concept. The fact that a gating circuit may be present in the prior art is not sufficient to establish inherency. The Examiner must show (not just merely state) that a termination of prefetching necessarily requires a gating circuit. In other words, the Examiner must prove the following statement P:

P ≡ if there is a termination of prefetching, then a gating circuit is required.

Applicants take the liberty to prove that P is false as follows. The above statement is in the form "if s then t". This predicate calculus form is equivalent to "if not t, then not s".

Therefore, assuming that the Examiner were successful in proving P, that proof would lead to the following result.

Q ≡ If a gating circuit is not required, then there is not a termination of prefetching.

It is clear that the statement Q is absurd and is totally false because there are many cases that a gating circuit is not required but a prefetching may still be terminated. Since Q is false, and Q is equivalent to P, it leads to P being false.

2) The prior art reference discloses a derived prefetch address, not a prefetch address.

In the Office Action, the Examiner states that "a derived prefetch address is a prefetch address". If this is true, what is the reason to call it a "derived" prefetch address? As argued in the previous response, Lopez-Aguado discloses that the derived prefetch address is the sum of a stride and an extracted physical address (Lopez-Aguado, col. 7, lines 18-20). As the Examiner may be aware, a 102(b) rejection requires that the prior art reference must show the identical invention in as complete detail as is contained in the claim. See, for example, Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989). Here, the derived prefetch address is not the same as the prefetch address.

3) The prior art reference does not disclose matching with the most recent prefetch address.

In the Office Action, the Examiner states that "since it is determined if the derived prefetch address is already in the queue, it is determined if it matches at least P addresses in the queue." First, as argued above, Lopez-Aguado merely discloses derived prefetch address, not prefetch address. Second, Lopez-Aguado does not disclose that the address in the queue represent the most recent access requests from a processor. Third, determining if the derived prefetch address is already in the queue is not, expressly or inherently, equivalent to matching at least P prefetch address in the queue.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §102(b) be withdrawn.

Rejection Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 6-10 and 16-30 under 35 U.S.C. §103(a) as being unpatentable over Lopez-Aguado in view of U.S. Patent No. 6,134,633 issued to Jacobs ("Jacobs"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Applicants reiterate the arguments set forth in the previously filed Response to the Office Action.

Jacobs discloses a prefetch management in cache memory. A prefetch memory supports discarding of prefetch addresses that are associated with operations executed by the processor such as by employing a fully associative prefetch memory when comparing addresses of cache access operations to the addresses held in the prefetch memory (Jacobs, Col. 7, lines 4-10).

Lopez-Aguado and Jacobs, taken alone or in any combination, does not disclose, suggest, or render obvious (1) a gating circuit to disable an access request to a memory when the access request is canceled and (2) a plurality of comparators to compare the current prefetch address with each of the stored prefetch address. There is no motivation to combine Lopez-Aguado and Jacobs because neither of them addresses the problem of gating the access request to disable the access request to a memory. There is no teaching or suggestion that a gating circuit or a plurality of comparators is present. Lopez-Aguado and Jacobs, read as a whole, does not suggest the desirability of gating the access request. Furthermore, Jacobs merely discloses using a fully associative prefetch memory when comparing the addresses of cache access operations, not comparing a current prefetch access request with each of the stored prefetch address.

Therefore, Applicants believe that independent claims 1, 11, and 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §102(b), and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 01/16/2004 By _____

Thinh V. Nguyen
Reg. No. 42,034
Tel.: (714) 557-3800 (Pacific Coast)

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025

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